POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2018
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.

1. a) Explain different stages of computer evolution with reference of generation of computer.
   b) Explain instruction cycle state diagram with interrupt.
2. a) How overflow be detected in computer? Verify the operation (7) / (-3) using signed 2's complement method.
   b) Compare and Contrast between micro-program and hardwired control unit. Explain the micro program sequencer with example.
3. a) What is interrupt cycle? Explain how instruction be processed with interrupt in computer along with necessary diagram.
   b) What is m-way interleaving? Explain different types of memory interleaving.
4. Consider a system with main memory (MM) consisting of 8K blocks, a cache memory consisting of 256 blocks and a block size of 16 words- what will be the word field, block filed and Tag field length? How many bits are there in main memory address? If the system uses direct mapping and associative mapping techniques.
   b) What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks.
5. a) Assume that pipeline has K=8 segment and execute n=125 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline.
   b) What type of hardware and software performance issues are seen in multi-core computers? Explain.

6. a) Explain different interconnection structures in multiprocessors.
   b) What is cache coherence problem? Explain MESI protocol for solving cache coherence problem.
7. Write short notes on: (Any two)
   a) RISC vs. CISC
   b) Hardware Description language (HDL)
   c) Logic Microoperation

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2018
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the characteristics of computer system? Draw and explain the basic computer organization in detail. 8
   b) What is RTL? Explain it when data transfer takes place between one and four bit register. 7
2. a) How a floating point number is represented in computer system? Verify the operation (9) x (-2) using signed magnitude data 8
   b) What is sequencer? Draw and explain the micro programmed control unit in detail. 7
3. a) What is instruction cycle? Write the necessary micro-operations for fetch, decode, indirect and interrupt cycles. 8
   b) What is mapping? What are the different cache memory mapping technique? 7
4. a) What is DMA? Explain why DMA is used instead of interrupt driven and programmed I/O? 7
   b) What is instruction pipeline? Explain 3-segment instruction pipelining used in RISC computer. 8
5. a) How a computer system can be classified according to flyn's? Design an arithmetic pipeline to speed up the computer to solve the expression $A_i * C_i + D_i$ for i=0, 1,2,3,4. 8
   b) What are the function of ISR? Explain how interrupt are processed in computer system. 7
6. a) How floating point number can be added or subtracted using pipelining techniques? 8
   b) What are different interconnection structure when there are multiple 7

CPUs?

7. Write short notes on: (Any two)
   a) Alternative Chip Organization
   b) Types of registers
   c) Control memory organization and mapping logic

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2019
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.

1. a) Explain the functional view of the computer system with reference to each component. 8
   b) How data can be transferred between registers? Explain in detail. 7
2. a) Describe the arithmetic and logic circuit with its appropriate block diagram. 7
   b) Multiply $(14)_{10}$ and $(3)_{10}$ using unsigned binary multiplication method with data flow diagram. 8
3. a) Perform (-5) *(-3) using the Booth multiplication algorithm. 8
   b) Compare single and two address field addressing techniques used in micro-programmed implementation of control unit. 7
4. a) Does hardwired implementation of Control Unit makes control unit fast or slow explain? Mention disadvantages of Hardwired implementation. 8
   b) What is associative memory? How match logic works for associative memory? 7
5. a) Define DMA. Explain DMA controller with different DMA transfer modes. 7
   b) Explain the advantages of pipelining in the multiprocessor system. Describe the instruction pipeline with examples. 8
6. a) Why cache coherency occur in multiprocessor system? What are the various ways to troubleshoot the problem? 8
   b) Explain Flynn's classification of computer system. 7
7. Write short notes on: (Any two) 2×5
   a) Optical disk
   b) RISC Vs CISC
   c) Multi Core Organization

POKHARA UNIVERSITY

Level: Bachelor | Semester: Spring | Year : 2019
Programme: BE | Full Marks: 100
Course: Computer Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain the different evolutionary milestones in development of computer system. 7
   b) What are the different types of register used in computer system, explain with examples. 8
2. a) Write the algorithm and perform multiplication of 9*-3 using booth algorithm. 8
   b) Differentiate between micro programmed control and hardwired control unit? What are the techniques used to sequence microinstructions.
3. a) What is instruction cycle? Explain various sub cycle of instruction cycle with micro-instructions involved in each sub cycle.
   b) Define virtual memory. Explain address mapping using pages in virtual memory.
4. a) Explain how redundancy is obtained in RAID, with reference to any two RAID levels. What is the application of RAID?
   b) Explain with an example, how effective address is calculated in Direct, Register indirect, Relative and Index addressing modes. (Assume necessary data if you need)
5. a) What is mean by pipelining? Explain in brief about RISC pipelining?
   b) What is cache coherence problem? Explain methods of solving cache coherence problem.
6. a) What are the various interconnected structure used for multiprocessor system? Explain them.
   b) Briefly explain the different performance issues in Hardware.
7. Write short notes on: (Any two) 2
   a) Register Transfer language (HDL)
   b) Future trends in computer
   c) Instruction pipelining

POKHARA UNIVERSITY

Level: Bachelor
Programme:B E
Course:Computer Architecture

Semester:Fall

Year : 2020
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.
The figures in the margin indicate full marks.
Attempt all the questions.

1. a) Differentiate Computer Organization and architecture. Explain the various addressing modes. 8
   b) Define RTL. Explain about BUS and Memory transferin RTL. 7
2. a) Explain different types of registers used in computer system. What is use of register in computer system? 7
   b) Perform multiplication -13*7 using Booth's Algorithm. 8
3. a) What are the various number representation method in computer system? 7
   b) Explain block diagram of micro programmed control organization and write down its advantages. 8
4. a) Explain associative and set-associative mapping in cache memory? 8
   b) Define an interrupt with its classes in detail. Also explain about interrupt driven I/O. 7
5. a) What is pipelining hazards? Explain structural and data hazard and its solution 7
   b) What is cache coherence problem? Explain software and hardware solution of cache coherence problem. 8
6. a) Write about parallelism in computer system. Explain about symmetric multiprocessor in detail. 7
   b) Explain about the various Hardware Performance issues in Multicore Computers. 8

7. Write short notes on: (Any two)

a) Shift Micro operations

b) Magnetic tape and disk

c) Differentiate between RISC and CISC.

CA-I-F-22

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2022
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Discuss the term Computer Architecture. Explain IAS computer architecture with detailed diagram.
   b) Define addressing mode. Explain different addressing modes with appropriate figures and example of each. 7
2. a) Define RTL. How data can be transferred between registers. Explain. 8
   b) Define Instruction cycle. What are the different states in an instruction cycle? Also explain fetch cycle, decode cycle, execute cycle and indirect cycle. 8
3. a) Draw the flowchart for Booth's Algorithm. Use the algorithm for binary multiplication of (-12) and (-9). 8
   b) Explain single and two address field sequencing techniques in micro programmed control unit. 7
4. a) Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. 7
   b) What is memory hierarchy? Explain with reason why do we need multilevel memory hierarchy? 7
5. a) Explain various communication techniques for I/O devices. 8
   b) Differentiate between various mapping techniques when main memory data is to be mapped into cache memory. 7
6. a) What is power efficient processor? Explain dual core processor with respect to quad core processor. 8
   b) Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems. 7
7. Write short notes on: (Any two) 2×5
   a) RISC vs. CISC
   b) Vector processors and Array processors
   c) BCD Adder

POKHARA UNIVERSITY

Level: Bachelor | Semester:Spring | Year : 2024
Programme: BE | Full Marks:100
Course: Computer Architecture (New) | Pass Marks: 45
Time :3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by addressing modes? Explain different addressing modes with suitable examples and diagrams. 7
   b) Evaluate X = (M*N) + (P*Q) using three, two, one and zero address instructions. 8

   OR

   Differentiate between computer architecture and computer organization. Briefly explain the future trends in computer.
2. a) Write the structure of VHDL programming and write code for full adder using component. 8
   b) Registers in CPU perform two major roles. What are the various register involved to fulfill the roles? 7
3. a) Define control memory. Explain the working of microprogrammed control unit. Differentiate between Horizontal and Vertical microprogrammed control unit. 8

   OR

   Why microinstruction sequencing is important? Explain variable address field sequencing techniques with necessary block diagram.
   b) Perform unsigned binary multiplication of 17*4 using Booth's algorithm. 7
4. a) What are the pipelining hazards? How can they be removed? 8
   b) What is mapping in memory? What are the various mapping techniques? Explain in detail. 7
5. a) Briefly explain the various memory storage devices of memory organization. 8
   b) DMA overcomes the drawback of programmed I/O and interrupt driven I/O. How can you clarify the statement? 7
6. a) How can you achieve Parallelism in Uniprocessor System? Explain about Flynn's Classification of Parallel Processors. 8

b) What are the common hardware-related and software-related performance issues that can arise in multi core systems and how do they impact computational efficiency? 7

7. Write short notes on: (Any two) 2×5

a) Floating point arithmetic

b) Register Windowing

c) GPU and TPU

POKHARA UNIVERSITY

Level: Bachelor | Semester:Spring | Year : 2024
Programme: BE | Full Marks:100
Course: Computer Architecture (New) | Pass Marks: 45
Time :3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by addressing modes? Explain different addressing modes with suitable examples and diagrams. 7
   b) Evaluate X = (M*N) + (P*Q) using three, two, one and zero address instructions. 8

   OR

   Differentiate between computer architecture and computer organization. Briefly explain the future trends in computer.
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   Why microinstruction sequencing is important? Explain variable address field sequencing techniques with necessary block diagram.
   b) Perform unsigned binary multiplication of 17*4 using Booth's algorithm. 7
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   b) What is mapping in memory? What are the various mapping techniques? Explain in detail. 7
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   b) DMA overcomes the drawback of programmed I/O and interrupt driven I/O. How can you clarify the statement? 7
6. a) How can you achieve Parallelism in Uniprocessor System? Explain about Flynn's Classification of Parallel Processors. 8

   b) What are the common hardware-related and software-related performance issues that can arise in multi core systems and how do they impact computational efficiency? 7
7. Write short notes on: (Any two) 2×5
   a) Floating point arithmetic
   b) Register Windowing
   c) GPU and TPU

POKHARA UNIVERSITY

Level: Bachelor | Semester:Spring | Year : 2024
Programme: BE | Full Marks:100
Course: Computer Architecture | Pass Marks: 45
Time :3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Discuss the term Computer Architecture. Explain IAS computer architecture with detailed diagram.	7
	b)	Briefly explain the terms instruction set, addressing modes and instruction formats.	8
2.	a)	What is register transfer? Briefly explain arithmetic and Logical micro-operation.	7
	b)	Explain about the internal structure of processor also explain the design principle for modern system.	8
3.	a)	Describe the steps involved in Booth's algorithm and provide an example to multiply unsigned binary number.	8
	b)	What are the significances of encoded control words in vertical microprogrammed control unit? Differentiate between hardwired and microprogrammed control unit.	7
4.	a)	Explain direct mapping and associative mapping in cache memory with necessary diagrams.	8
	b)	What is memory hierarchy. Explain with reason why do we need multilevel memory hierarchy?	7
5.	a)	What are the drawbacks of Programmed I/O and interrupt driven I/O? Explain how DMA overcomes these drawbacks.	7
	b)	Prove that "Speedup factor for pipelined processor is equal to number of stages in pipeline." Assume that pipeline has K = 6 segment and execute n = 120 tasks in a sequence. Let the time taken to process the sub-operation in each segment is 30ns. Calculate the speedup ratio.	8
6.	a)	Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems.	8
	b)	Differentiate dual core and quad core processor. What are the software performance issue that arise in multicore architecture?	7

b) Prove that "Speedup factor for pipelined processor is equal to number of stages in pipeline." Assume that pipeline has K = 6 segment and execute n = 120 tasks in a sequence. Let the time taken to process the sub-operation in each segment is 30ns. Calculate the speedup ratio. 8

6. a) Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems. 8

b) Differentiate dual core and quad core processor. What are the software performance issue that arise in multicore architecture? 7

2×5

7. Write short notes on: (Any two)
   a) BCD Adder
   b) VHDL and its advantages
   c) Array Processors

POKHARA UNIVERSITY

Level: Bachelor | Semester : Spring | Year : 2023
Programme: BE | Full Marks: 100
Course: Computer Architecture | Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Differentiate between Computer Organization and Computer Architecture. Explain the functional view of the computer with reference to each component.	8
	b)	Define RTL. Explain about Bus and Register transfers in RTL.	7
2.	a)	Explain different types of registers used in Computer System with examples. What is the use of registers in Computer System?	7
	b)	Perform -15 *6 using Booth's algorithm.	8
3.	a)	Explain the restoring division algorithm with flowchart.	8
	b)	Explain the working principle of Micro-programmed implementation of control unit. Why is it slower than Hardwired Control Unit?	7
4.	a)	What is associative memory? How read /write operation takes place in associative memory?	7
	b)	As we know cache memory size is smaller than main memory, how is it possible to map main memory data into cache memory? Explain in detail.	8
5.	a)	How Interrupt driven I/O differ from programmed I/O? Explain with necessary diagram.	7
	b)	How instruction pipelining supports in parallelism? Explain.	8
6.	a)	Cache coherence problem arise in multiprocessor system and must be resolved. Justify this statement.	8
	b)	What are the performance issues that arise in multicore computers?	7
7.		Write short notes on: (Any two)	2×5
	a)	Control unit.	
	b)	RISC VS CISC	
	c)	Flynn's Classification	